

REMARKS

Reconsideration of the present application is respectfully requested.

Claims 1-30 previously presented for examination remain in the application.

Claims 1, 11 and 21 have been amended not for patentability reasons, but to improve clarity. No new claims have been added and no claims have been canceled.

Claims 21 and 27 stand objected to due to informalities. In particular, it is stated that the word "processor" is missing after the word "host" in claim 21 at line 3. Claim 21 has been amended as indicated to correct this informality.

It is further stated that for each of claim 21, line 4 and claim 27, line 6, the word "an" must be replaced with the word "a." Applicant respectfully traverses this objection. At each of these locations, the word "an" precedes the acronym "SMI." "SMI, when spoken is pronounced "ess emm eye." Therefore, the word "an" properly precedes "SMI" and no correction should be required. Applicant respectfully requests withdrawal of the objection.

Claims 11 -20 stand rejected under 35 U.S.C. § 101 as being considered to be directed to non-statutory subject matter either directly or as dependent claims. In particular, the Office Action states that claims 11 and 17 are not limited to tangible embodiments. The position taken in the Office Action is that program or code segments transmitted by a computer data signal embodied in a carrier wave, processor readable media including a radio frequency (RF) link, transmission media such as air, electromagnetic, RF links are intangible, and therefore non-statutory. Applicant respectfully traverses this rejection.

More specifically, applicant respectfully submits that the all of the claimed media are tangible and therefore the associated claims cover statutory subject matter for at least the following reasons.

Current laws, legal precedent and Examiner Guidelines clearly allow claims in the form of computer readable medium, as recited in claims 11 and 17. See *In re Beauregard*, 35 USPQ2d 1383 (CAFC 1995). Further, current laws, legal precedent and Examiner Guidelines clearly allow claims directed to carrier waves and other media recited in the Office Action.

For example, in the Examination Guidelines For Computer-Related Inventions as available on the USPTO web site at URL

http://www-uspto-gov/web/offices/pac/dapp/mpep_examguide.html. (where periods have been replaced with dashes to avoid unintentional insertion of hyperlinks), example claim 13 in the document at URL <http://www-uspto-gov/web/offices/pac/dapp/pdf/compenex.pdf> is clearly directed to a computer data signal embodied in a carrier wave (see pg. 37) and provided as an example of statutory subject matter (see e.g. pages 39 "...the data signal does not occur as a natural phenomenon"..."absent object evidence to support the position that the "data signal" is a natural phenomenon, such a position would be untenable." and page 45 "...the computer medium is embodied on a computer-readable medium—the carrier wave. Thus, claim 13 is a statutory article of manufacture claim." Based on at least the foregoing, the Examiner guidelines clearly show that this type of claim is a *statutory computer program embodied on a computer-readable medium*, where the computer-readable medium is a carrier wave.

Thus, the alternative description of machine accessible media as described at paragraph [0016] in the Specification, clearly describes statutory subject matter.

Further support for this position may also be found in the form of legal precedent. For example, while it is asserted in the Office Action that a signal or "carrier means" is *non-statutory* because it is not "in a tangible medium," there is legal precedent that shows that the view that there is nothing physical (i.e., tangible) about signals is incorrect.

"These claimed steps of "converting", "applying", "determining", and "comparing" are physical process steps that transform one physical, electrical signal into another. The view that "there is nothing necessarily physical about 'signals'" is incorrect. *In re Taner*, 681 F.2d 787, 790, 214 USPQ 678, 681 (CCPA 1982) (holding statutory claims to a method of seismic exploration including the mathematically described steps of "summing" and "simulating from"). The Freeman-Walter-Abele standard is met, for the steps of Simson's claimed method comprise an otherwise statutory process whose mathematical procedures are applied to physical process steps."

Arrhythmia Research Technology Inc. v. Corazonix Corp. 22 USPQ2d 1033, 1038 (CAFC 1992).

"Appellants' claims are not in our view merely directed to the solution of a mathematical algorithm. Though the claims directly recite an algorithm, summing, we cannot agree that appellants seek to patent that algorithm in the abstract. Appellants' claims are drawn to a technique of seismic exploration which simulates the response of subsurface earth formations to cylindrical or plane waves. That that technique involves the summing of signals is not in our view fatal to its patentability. Appellants' claimed process involves the taking of substantially spherical seismic signals obtained in conventional seismic exploration and converting ("simulating from") those signals into another form, i.e., into a form representing the earth's response to cylindrical or plane waves. Thus the claims set forth a process and are statutory within §101.

For at least the foregoing reasons, applicant respectfully submits that claims 11 and 17 cover statutory subject matter and, therefore, so do dependent

claims 12-16 and 18-20, which depend from and further limit claims 11 and 17, respectively.

Claims 3, 4, 13 and 23 stand rejected under 35 U.S.C. § 112, second paragraph as being considered to be indefinite. In particular, it is stated that claims 1, 11 and 21 include alternative language used to describe updating the performance state structure using either a processor performance table or a default table while claims 3, 13 and 23 imply the presence of both.

Applicant agrees with the statement in the office action that claims 1, 11 and 21 use alternative language to describe updating the performance state structure using either a processor performance table or a default table and also with the statement that claims 3, 13 and 23 imply the presence of both.

Applicant disagrees, however, with the statement that these are contradictory.

For some embodiments, for example, the performance state structure may be updated with either the processor performance table or the default table even where both of them are present.

It is stated in the Office Action that, if the applicant desires the presence of both the processor performance table and the default table, claims 1, 11 and 21 need to be modified to account for that. Applicant respectfully traverses this position.

Claim 1 is directed to a method for which the actions are clearly set forth in the claims including an action of updating a performance state structure using one of a processor performance table and a default table. Claim 11 is directed to

an article of manufacture that performs a process, which is also similarly clearly set forth in the claims and claim 21 is directed to a system including a memory to store an SMI handler that performs a process that is also clearly specified in the claims. There is no requirement for any of these claims to further specify the presence of both a processor performance table and a default table and there is no inconsistency in the way the claims are presently presented.

Applicant respectfully submits that the claims as presented meet the requirements of 35 U.S.C. § 112, second paragraph.

Claims 1, 6, 11 and 16 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over U.S. Patent No. 6,721,892 to Osborn et al. ("Osborn") in view of U.S. Patent No. 5,958,058 to Barrus ("Barrus").

Claim 1 includes the limitations

reading a performance information associated with a processor;
attempting to locate a processor performance table that corresponds to the performance information, the performance table including a plurality of performance parameters to control performance of the processor; and
updating a performance state (PS) structure using one of the processor performance table and a default table.

(Claim 1)(emphasis added).

Applicant respectfully submits that Osborn and Barrus, alone or in combination, do not teach or suggest the claimed features of applicant's invention including at least reading a performance information associated with a processor and locating a processor performance table that corresponds to the performance information.

Osborn discloses an approach for dynamic performance adjustment of computation means. According to Osborn, a dynamic performance adjustment control circuit adjusts the clock frequency and voltage at which a logic circuit operates to a relatively greater frequency and voltage or relatively lesser frequency and voltage depending on the tasks to be performed and the duration in which they're required to be performed. (Osborn, Abstract).

For one approach, the dynamic performance adjustment circuit of Osborn receives a performance indication signal indicating the performance requirements of a functional circuit for a particular task. The dynamic performance adjustment control circuit then makes an adjustment to a performance input signal and/or a support signal to functional circuit to dynamically adjust. (Osborn, col. 5, lines 54 – 61). For one implementation, the dynamic performance adjustment control circuit determines an optimized clock rate and power supply voltage based upon the task to be performed by the logic circuit using a hash table to determine appropriate performance controls and support functions. In the example given, a single table is used to track seven different tasks and provides a correlation to their associated performance and support requirements in terms of a single entry or setting per task. (Osborn, col. 9, line 53 – col. 10, line 22, Figure 6). An example embodiment of Osborn applies to adjusting the performance of a modem processor based on communication rate. (col. 10, line 37 – 52).

Assuming, for purposes of argument, that a particular communication rate of a modem processor corresponds to the performance information set forth in

claim 1, Osborn does not teach or suggest attempting to locate a processor performance table corresponding to the communication rate. Osborn discloses only one table with entries corresponding to particular rates.

Further, as admitted in the Office Action, Osborn does not teach or suggest updating a performance state structure using one of a default table and a processor performance table.

A combination of Barrus with Osborn, were such a combination to be made, does not remedy these deficiencies. Barrus discloses a user-selectable power management interface with application threshold warnings that includes allowing a user to adjust the hardware performance settings of particular hardware devices on a computer in order to extend battery life (Barrus, Abstract).

According to Barrus, as the user adjusts the hardware settings, the computer notifies the user whether the performance of any software applications loaded on the computer would be adversely affected by the hardware settings. For one approach, the computer automatically detects all software applications on the computer and inputs the minimum operating requirements for each application into a data structure. As the user manipulates the hardware power settings, the computer accesses the data structure and compares it to the power settings. The computer then notifies the user if the power settings are set below desired levels for any of the applications on the computer. (Barrus, Abstract).

While Barrus discloses that a table may be provided for each application running on a computer system (col. 4, line 62 – col. 6, line 3), they are all loaded into the data structure and are not located based on performance information.

For at least these reasons, a combination of Osborn and Barrus, were such a combination to be made, would still fail to teach or suggest the claimed features of applicant's invention.

Independent claims 7, 11, 17, 21 and 27 include similar limitations.

Claims 2-6, claims 8-10, claims 12-16, claims 18-20, claims 22-26 and claims 28-30 depend from and further limit claims 1, 7, 11, 17, 21 and 27, respectively and thus, should also be found to be patentably distinguished over Osborn and Barrus, alone or in combination, for at least the same reasons.

Claims 2 and 12 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Osborn and Barrus and further in view of U.S. Patent No. 5,796,939 to Berc et al. ("Berc").

Claims 21 and 26 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Osborn and Barrus and further in view of U.S. Patent No. 6,112,164 to Hobson et al. ("Hobson").

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Osborn in view of Barrus, Berc and Hobson.

Each of these claims depends from and further limits a claim with similar features as argued above in reference to claim 1. As argued above in reference to claim 1, Osborn and Barrus, alone or in combination, fail to teach or suggest attempting to locate a processor performance table based on a performance information and updating a performance state structure with the located table.

Applicant respectfully submits that Berc and Hobson also fail to remedy the deficiencies of Osborn and Barrus, alone or in combination. Neither Berc nor

Hobson teach or suggest attempting to locate a processor performance table that corresponds to the performance information, the performance table including a plurality of performance parameters to control performance of the processor, and updating a performance state (PS) structure using one of the processor performance table and a default table as set forth in claim 1. Thus, any combination would also fail to teach or suggest such features.

As discussed above, independent claims 7, 11, 17, 21 and 27 include similar limitations to claim 1. Claims 2-6, claims 8-10, claims 12-16, claims 18-20, claims 22-26 and claims 28-30 depend from and further limit claims 1, 7, 11, 17, 21 and 27, respectively and thus, should be found to be patentably distinguished over Osborn, Barrus, Berc and Hobson alone or in any combination, for at least the same reasons.

Applicant gratefully acknowledges the allowance of claims 7-10 and 27-30. Applicant further gratefully acknowledges that claims 3-5, 13, 17-19 and 23-24 would be allowable if rewritten to overcome the applicable objections and rejections and to include all of the limitations of the base claim and any intervening claims.

Based on the foregoing, applicant respectfully submits that the applicable objections and rejections have been overcome and claims 1-30 are in condition for allowance.

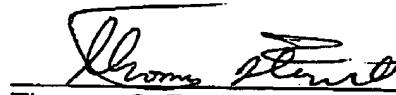
If the Examiner disagrees or believes that further discussion will expedite prosecution of this case, the Examiner is invited to telephone applicant's representative Cynthia Thomas Faatz at (408) 765-2057.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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